library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

entity Sumator\_flux is

port(

A : in BIT;

B : in BIT;

C : in BIT;

D : in BIT;

CI : in BIT;

X : out BIT;

Y : out BIT;

CO : out BIT

);

end Sumator\_flux;

--}} End of automatically maintained section

architecture Arhitectura of Sumator\_flux is

begin

-- enter your statements here --

x <= (not(b) and not(ci) and (a xor c)) or

(b and d and not(ci) and (a xnor c)) or

((a xor c) and not d and not(ci)) or

(not(b) and not(d) and ci and (a xor c)) or

(b and ci and (a xnor c)) or

(d and ci and (a xnor c));

y <= (b xor d) xor ci;

co <= (a and c and not(ci)) or

(b and c and d and not(ci)) or

(a and b and d and not(ci)) or

(a and ci ) or (c and d and ci) or

(b and c and ci);

end Arhitectura;